A holistic methodology that drives to process window entitlement and its application to 20 nm logic

Lalit Shokeen[a], Ayman Hamouda[a], Mark Terry[a], Dan J. Dechene[b], Stephen Hsu[b], Michael Crouse[b], Pengcheng Li[b], Keith Gronlund[b], Gary Zhang[b], [a]GLOBALFOUNDRIES, 400 Stone Break Extension, Malta, NY 12020, [b]ASML Brion, 4211 Burton Drive, Santa Clara, CA 95054, USA

ABSTRACT

Early in a semiconductor node's process development cycle, the technology definition is locked down using somewhat risky assumptions on what the process can deliver once it matures. In this early phase of the development cycle, detailed design rules start to be codified while the wafer patterning process is still being fine-tuned. As the process moves along the development cycle, and wafer processes are dialed-in, key yield improvement efforts focus on variability reduction. Design retargeting definitions are tweaked and finalized, and the use of finely tuned etch models to compensate for process bias are applied to accurately capture the more mature wafer process. The resulting mature patterning process is quite different from the one developed during the early stages of the technology definition.

In this paper we describe an approach and flow to drive continuous improvement in the mask solution (OPC and MB-SRAF) later in the process development and production readiness cycle stage. First, we establish the process window entitlement within the design-space by utilizing advanced mask optimization (MO) combined with the baseline process (i.e., model, etch compensation, and design retargeting). Second, gaps to the entitlement are used to identify and target issues with the existing OPC recipe and to drive continuous improvements to close these performance gaps across the critical design rules. We demonstrate this flow on a 20 nm contact layer.

Keywords: RET, Mask Optimization, Process window entitlement

1. INTRODUCTION

Technology development cycles for advanced technology nodes (i.e., 20 nm and below) can be broadly classified into three distinct phases: process definition, process development, and production readiness, each with varying degrees of flexibility in allowable changes to the process. Figure 1 shows a summary of the three different stages of technology development with different degrees of flexibility. While we briefly describe each of these hereafter, the major focus of this paper falls within the last two stages.

1.1 Process Definition

The process definition phase has the most flexibility to meet process requirements. During this phase of process development, design rules, patterning schemes, as well as key process specifics are being evaluated. In the context of resolution enhancement techniques/optical proximity correction (RET/OPC), it is in this stage where approaches such as source-mask optimization (SMO) [1] and design rule optimization (DRO) [2] are performed to obtain an optimal source pupil and retargeting shapes to meet process specifications. Design rules and standard cell designs are highly co-optimized in this stage through collaborative efforts often referred to as Design Technology Co-Optimization (DTCO).

1.2 Process Development

During the process development phase key technology identifiers such as the patterning scheme and key design rules have been determined in the context of RET/OPC, at this stage the majority of the focus is on accurately modeling the process (both post lithographic exposure, and post etch), as well as tuning the OPC solution to accurately print wafer targets while delivering maximum process window. The latter is accomplished through use of model based sub-resolution assist features (MB-SRAF) and the application of process window aware OPC solvers (such as PW-OPC).

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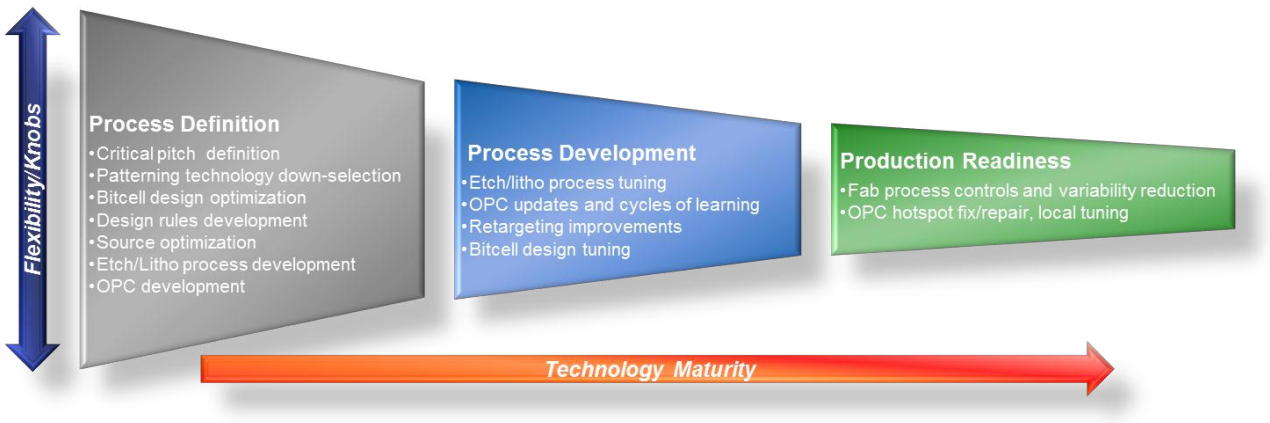


Figure 1. Process development flow for advanced technology nodes. From left to right, as technology development drives towards maturity, the flexibility to change the process (or knobs) is reduced.

1.3 Production Readiness

As the technology approaches maturity, process development focus shifts to yield ramp. Typical methods include identifying and fixing systematic yield detractors, as well as tightening process controls. On the lithographic scanner side, these process controls can include a number of techniques such as lens heating correction and scanner matching depending on the sensitivity and specs required by the process.

2. METHODOLOGY AND APPROACH

The major focus of this paper is later in the second and third stages of development where it is assumed that at this time, design rules, retargeting definitions and patterning technology has been locked in and an accurate process model is available. For the remainder of this paper, the term "Process Window Entitlement" is used to defined the maximum performance available (i.e., in terms of depth of focus) by changes induced via RET/OPC techniques.

2.1 Process Window Entitlement

Process window entitlement is defined as the targeted performance on a given process with a given set of constraints. This can be quantified in a number of ways. For the sake of simplicity, we define the process window entitlement (PW entitlement) for a given process as the depth-of-focus (DOF) in nanometers at 5% exposure latitude. With this definition and a stable wafer process, PW entitlement of an arbitrary geometry "*z*" is determined by computing the mask solution that maximized depth of focus. With this definition, the use of inverse lithographic solution (on a full-mask scale) can be used to approximate the process window entitlement for a given feature. It is assumed that such solutions cannot be used for this node in production environments on full designs due to practical OPC runtime considerations [1]. However, such approaches can be used to evaluate PW entitlement on systematic configurations and hotspots. Once the PW entitlement has been quantified for a given geometry, knowledge of the mask solution can be used to feedback into OPC recipe tuning. This approach allows us to focus on closing systematically large gaps where there is a high probability of reducing the gap with traditional OPC techniques. The aforementioned flow is described below.

2.2 Methodology Flow

A high-level flow diagram is shown in Figure 2. Here, design constructs such as logic standard cells, SRAM bit cells, systematic layouts and hotspots are fed into the system. These layouts are processed through two branches. The first upper branch in Fig. 2 quantifies the process window entitlement for a given geometry, while the lower branch quantifies the performance. A comparison is made on the performance of the two solutions. For geometries where the gap in performance between the two solutions is large, the existing recipe is tuned to improve the solution. Once the gap has been closed to within an acceptable tolerance, the performance is

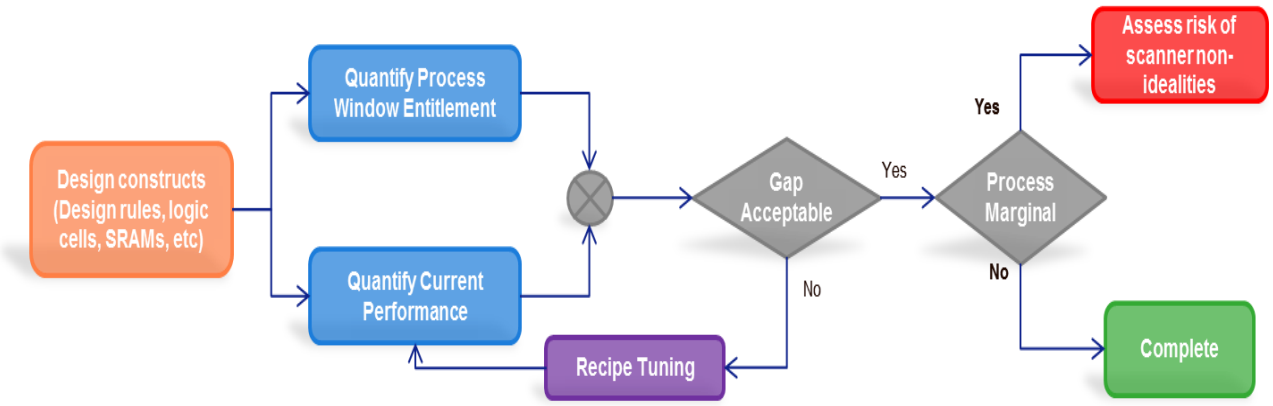


Figure 2. High level flowchart on methodology to close gap on process window entitlement

compared to the specifications required by the process. This portion of the flow is described in Section 3. For structures that have marginal process window, further analysis can be done on the geometry to assess the sensitivity to non-idealities for individual lithographic scanners within the fab. This portion of the flow is detailed in Section 4.

2.3 Tools Suite

The ASML Brion Tachyon software toolset is used to apply the methodology described above and is shown in Figure 3. Here, a calibrated FEM+ resist model is available and used to accurately simulate wafer level critical dimensions (CD). Geometries are taken from two sources: Systematic layout designed to assess ground rules and systematic deficiencies, and a pattern library containing known hotspots. The input geometries have been treated with all retargeting operations to provide the final lithographic target as input into the flow.

The targeted performance (or process window entitlement) is found by using Tachyon SMO's mask-only optimization, which provides a mask solution that also satisfies mask manufacturing rules. The "current performance" is obtained by running OPC using an existing recipe with Tachyon OPC+.

The output of both mask solutions is fed into an identical Tachyon LMC (process verification) recipe. The LMC recipe computes performance of both mask solutions based on a set of process assumptions. The set of process assumptions includes specs on the maximum tolerance on CD variation, and a set of process conditions describing the expected variation to be encountered by the process. The output of the two LMC runs summarizes a set of performance criteria which includes process variation bands (PV bands) and depth-of-focus (process window). A comparison is performed between both the mask optimization and existing mask solutions to identify the delta in performance. Geometries (or sets of geometries) with a large gap in performance (i.e., large gap in process window entitlement) are identified. Assist feature placement and OPC solution results from the mask optimization solution is fed back and used to tune the existing recipe (through both rule placement, MB-SRAF parameter tuning and OPC tuning). This process is continued until an acceptable gap has been achieved.

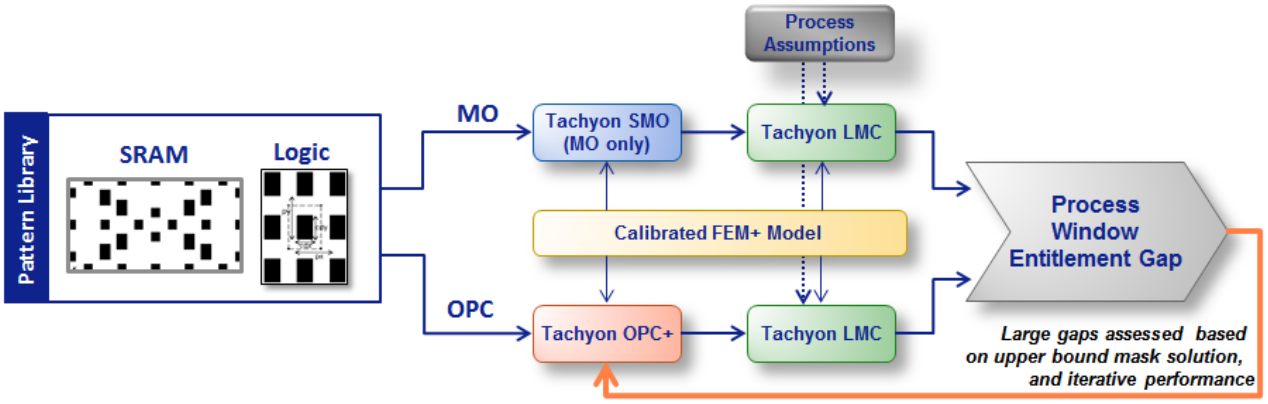
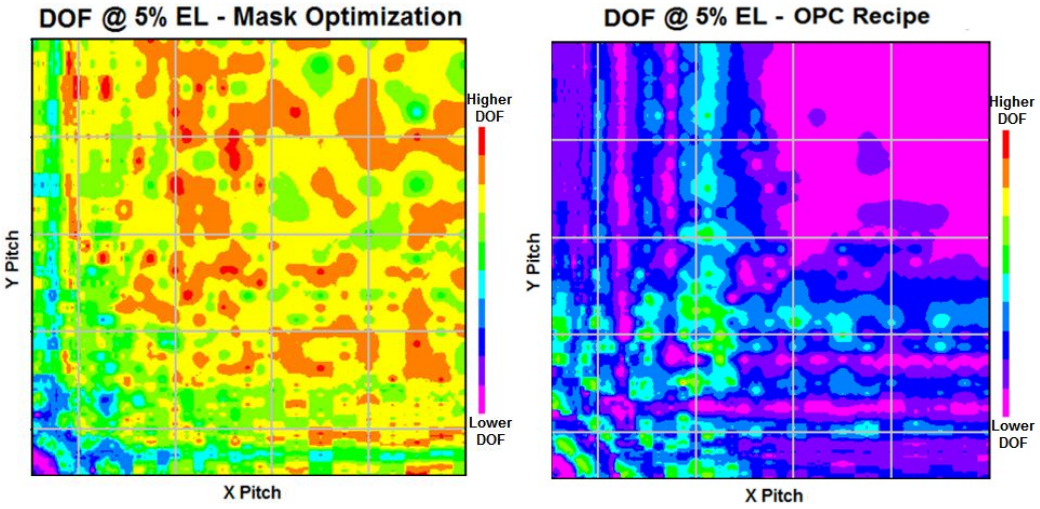


Figure 3. Detailed flow diagram of process window entitlement iterative loop

3. APPLICATION AND RESULTS

We apply the approach described in Section 2 on a 20nm via layer. An existing FEM+ model and OPC+ recipe are available. Process assumptions including necessary CD tolerance at litho, dose and focus control deliverable by the tool, and mask specifications are used to create an LMC recipe for evaluation. Retargeting is performed to obtain an overall lithographic target for evaluation. A case for systematic layouts and hotspots is presented as follows.



(a) (b)

Figure 4. Depth-of-focus performance of the systematic array. a) with full mask optimization and b) with existing recipe.

3.1 Systematic Layouts

Figure 4a) and b) show the DOF for one of a given set of layouts with a variation in x and y-pitch with full mask optimization and existing solution respectively while Figure 5 shows the delta between the two graphs shown in Figure 4. From the latter; we observe the regime for which there is opportunity for improvement (i.e., the gap is large). By comparing the mask results between both solutions, we observe additional assist feature placements with common run length on the edges which is not present with the existing solution. Using this information, we perform the following:

a) Tag polygon edges satisfying this systematic geometry
b) Tune MB-SRAF extraction and cleanup parameters limiting placement along these edges

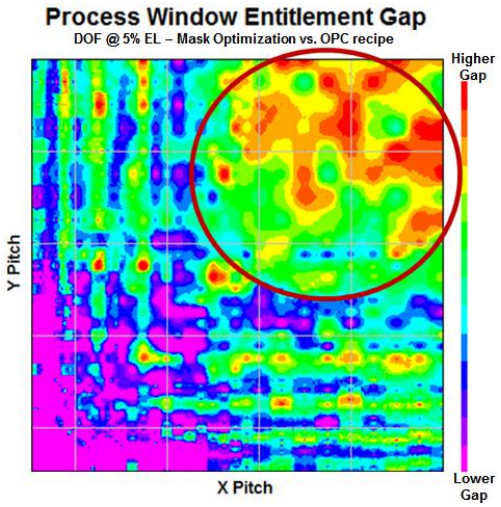


Figure 5. PW entitlement gap. Comparing Figs. 4a) and 4b) highlights systematic gaps to target tuning efforts. The scale from green to red shows regions with a small to large opportunity for improvement with tuning

Figure 6 shows the process window entitlement gap before and after recipe improvements. Figure 6a shows the large systematic gap has been improved via recipe tuning; while Figures 6b and 6c show the before and after solution.

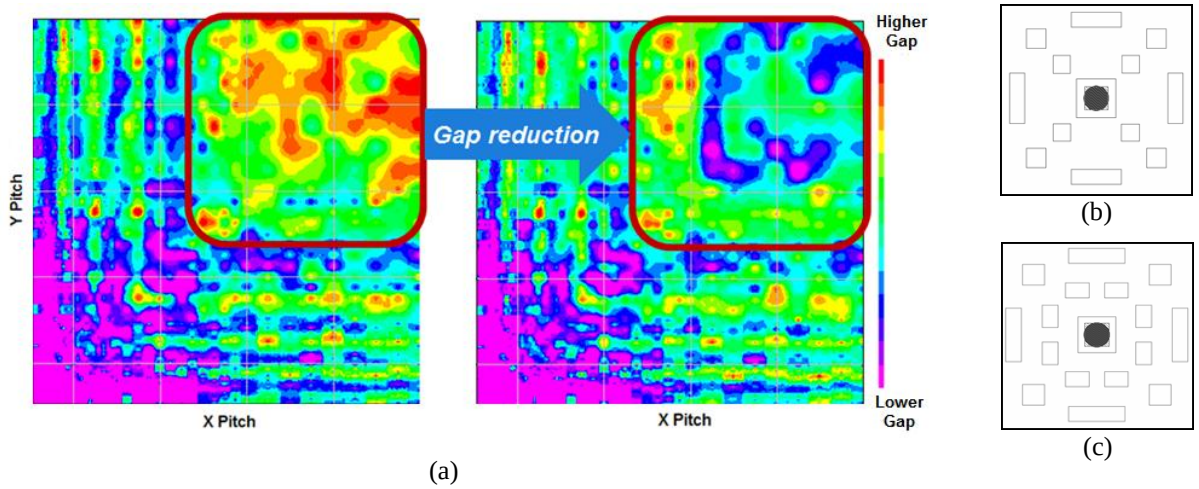


Figure 6. Recipe tuning on systematic array. a) overall process window entitlement gap before and after recipe optimization b) isolated SRAF solution before optimization, and c) isolated SRAF solution after optimization

Another case is shown in Figure 7. Here, we observe for bar structures, there is a large systematic region where process window is reduced. Further analysis of the full mask optimization solution shows that these structures benefit from support of the minor CD (shorter edge) with assist features. Here, we can isolate this systematic region with tagging and by filtering based on space. The model based assist parameters of the tagged structures are then tuned to provide additional support to the minor CD. Figure 8 shows the improvement obtained based on tuning. Figures 8a. and 8b. show the mask solution before and after tuning respectively. In Figure 8b, we can clearly observe the additional assists parallel to the minor bar CD. Figures 8c. shows the process window improvement from tuning the mask solution. From the EL/DOF plot, we can clearly observe a dramatic improvement in the common process window with the improved mask solution.

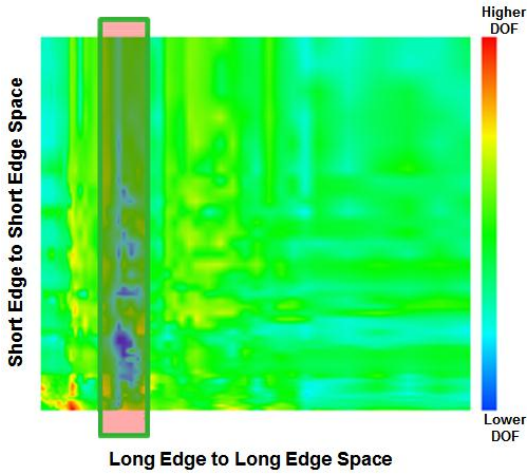
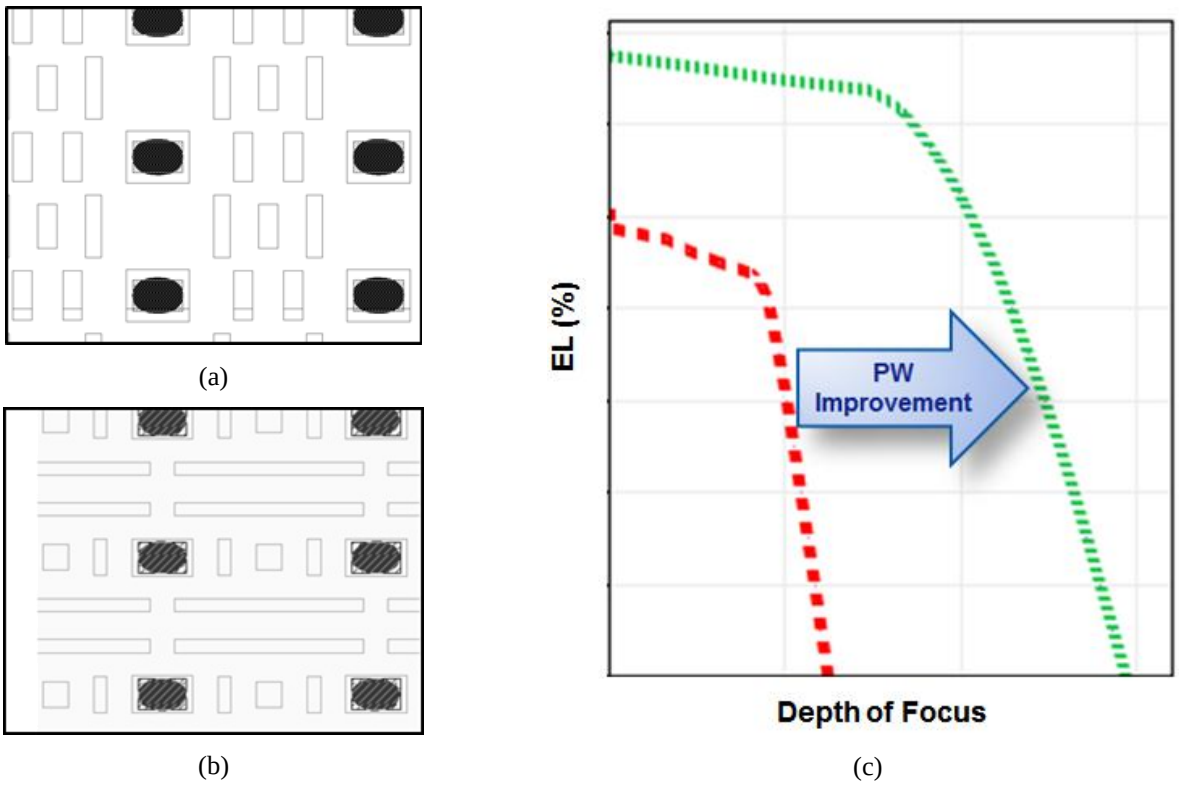


Figure 7. Another case of limited process window in a systematic configuration for bar structures



(a)

(b)

(c)

Figure 8. Systematically process window limited structures. Here a) shows the solution before recipe optimization, b) shows the solution after recipe tuning using full mask optimization results and c) shows the process window (PW) improvement before and after tuning.

The described approach above is applied to a number of systematic layouts within the design space.

3.2 Application to Random Logic Configurations

Once systematic performance gaps have been closed, the focus is on random logic hot spots including critical constructs, and SRAMs cells. Application to these specific constructs requires more specific approaches to identify and tag critical structures. In addition to traditional DRC, the use of pattern matching or upstream marker layers can also be used. Figure 9, we show an example of one such configuration and its current mask solution.

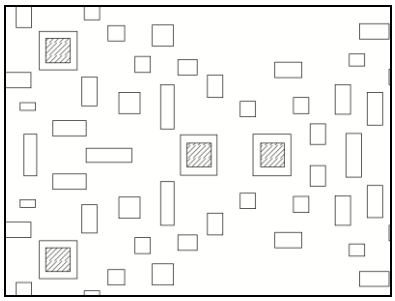
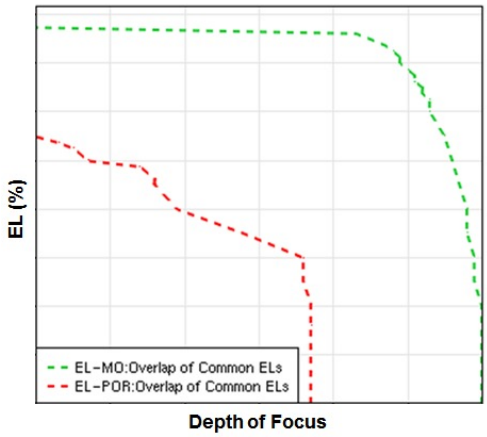


Figure 9. A non-systematic (logic) hotspot clip to be optimized.

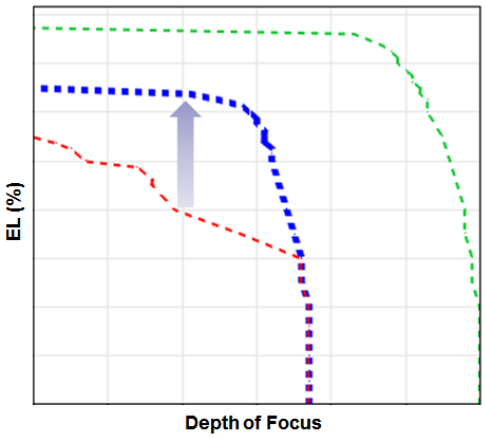
To apply the described methodology, the input litho targets are run through full mask optimization to evaluate the process window entitlement. By comparing both solutions, there are several key observations

- Assist density differences between the two solutions
- Assist placement differences between both solutions
- Target differences between both solutions (limiting common process window)

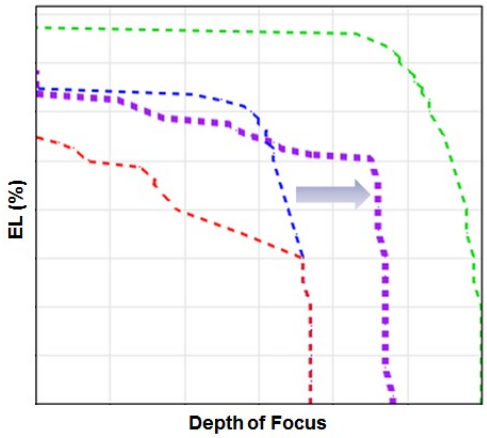
The process window entitlement gap is shown in Figure 10a. In round 1, we address the first and second observations by tuning the limiting MB-SRAF placement parameters and increasing the extraction search range for this hotspot. The results of the first round of optimization are shown in Figure 10b. We observe an improvement in the exposure latitude. Comparison of the round 1 solution still shows denser SRAF solution. To mimic this, we further reduce the limitations on SRAF to SRAF spacing which provides more flexible placement. The result of this tuning stage is shown in Figure 10c. Here, we see a clear improvement in the focus latitude. Comparing the results of round 2, we observe the common process window of the vertical and horizontal CD as the process window limiting features when compared to mask optimization solution. For round 3, we adjust the control points on the H and V edges separately to improve the common process window. The result of this third stage of tuning is shown in Figure 10d. Here, the overall focus latitude is improved with a small impact to the exposure latitude. At this stage, we consider the gap closed and progress to the next hotspot.



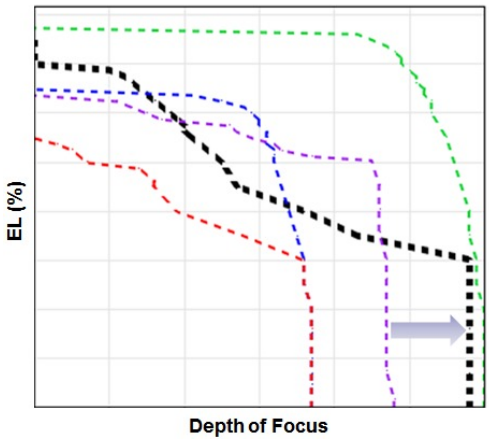
a) existing recipe gap



b) Following the initial round of tuning (MB-SRAF placement tuning)



c) Following the second round of tuning (further MB-SRAF placement tuning)



c) Following the third round of tuning (target optimization to improve H versus V common process window)

Figure 10. Iterative improvements with recipe optimization to drive to process window entitlement by applying learning from mask optimization

The approach is applied continuously on all hotspots within a level. Hotspots with a small process window entitlement gap are further analyzed on specific lithographic scanners within the fleet.

4. SCANNER SPECIFIC EVALUATION

Typically, resist models for OPC are calibrated using an average model of the process (i.e., an average of the lithographic scanners within the fleet). However, features with small process window may be more susceptible to non-idealities introduced by one or more of scanners within the fleet. Following the improvements described in Section 3, there may still exist some configurations with a small process window entitlement gap that are marginal in terms of process window performance. For example, examining Figures 4 and 5, we observe some semi-dense configurations where a) process window is lower and b) the process window entitlement gap is small. For these configurations, the impact of individual scanner non-idealities of specific scanners within the fleet can be examined to determine if there is any impact to these features.

The assessment of scanner specific non-idealities is performed using the flow shown in Figure 11. Here a scanner specific model is a snapshot at a specific time. Non-idealities including abberations, measured source pupil, mechanical stage dynamics and measured laser bandwidth can be used to create a scanner specific FEM+ model. We note however that the scanner specific model is not used to perform OPC, rather this is still done with the existing OPC recipe (i.e., the average scanner model).

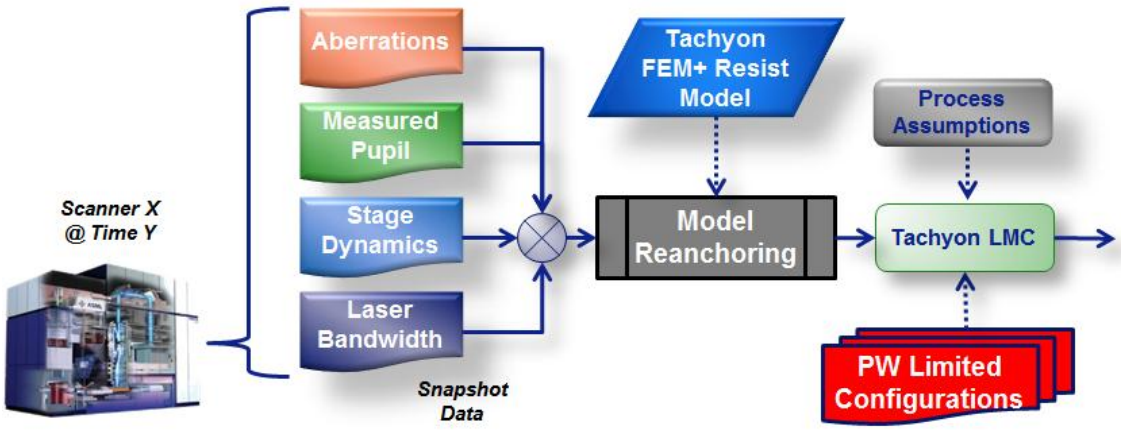


Figure 11. Flow chart on scanner specific FEM+ model generation and evaluation

The DOF for the average scanner, Scanner A and Scanner B is shown in Figure 12 for select orthogonal configurations from the test case shown in Figure 4. For these structures, we observe several key findings. First, the performance of the two scanners on these structures has very little negative impact on the limiting structure (i.e., the semi-dense pitch configuration). Second, we actually observe some small improvement in process window for some configurations versus the average scanner. The rationale here is as follows. OPC is performed with the average scanner model, while simulation is performed with individual models. While models utilize the same dose anchor, structures outside the anchor could experience a small dose offset (i.e., print slightly off nominal) due to variations in aberration and stage dynamics. For focus sensitive structures, the slight increase in nominal CD can actually marginally increase the process window of this structure (i.e., similar to how process window OPC for contacts prints slightly larger than nominal).

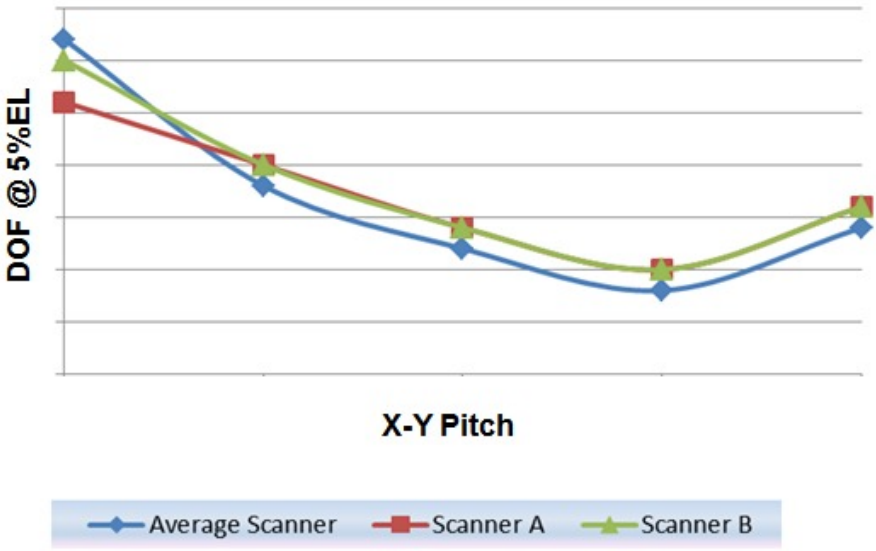


Figure 12. Performance of semi-dense orthogonal configurations on the average scanner (i.e., existing FEM+ model) and two specific scanners a given time.

For configurations that are shown to be sensitive to one or more specific scanners, there are several approaches that can be taken. For example, Pattern Matcher Full Chip (PMFC) could be employed. PWO can be used combined with focal maps to improve common process window by tuning focus. If a specific scanner shows high sensitivity, PMFC can be used to reduce scanner to scanner variation.

5. CONCLUSION

We presented a holistic approach that can be used to drive towards meeting process window entitlement in later stages of technology development. The use of full mask optimization was employed to identify systematic and random logic configurations with a large process window entitlement gap for targeted recipe improvements. Learning was iteratively fed back to improve the existing OPC recipe. Configurations with little to no entitlement gap were also found with this method and we showed that further analysis can be performed to better understand if any sensitivity on specific scanners when considering scanner non-idealities. A subset of results was shown demonstrating this approach on a 20nm logic layer.

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